Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.108”**

**.125”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size = .020 x .020”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .108” X .125” DATE: 12/10/19**

**MFG: INT’L RECTIFIER THICKNESS .010” P/N: IRFZ44VPOBF**

**DG 10.1.2**

#### Rev B, 7/1